SINGLE-CHIP TV NOISE REDUCTION
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ABSTRACT
This new noise reduction IC for consumer TV automatically adapts to the noise level, and achieves 3 dB improvement when used stand-alone. It doubles the gain of current NR designs when cascaded.

INTRODUCTION
Because TV sets are often used in areas where the reception conditions are less than optimal, inclusion of a noise reduction filter in the receiver adds an attractive feature. A new IC for economy TV 2-D spatial noise filtering has been designed. It includes a novel circuit for noise-level estimation for optimal filtering under varying reception conditions. When cascaded with commonly-available motion-adaptive temporal noise filters, a high quality 3-D concept for high-end TV results.

THE ALGORITHM
The newly developed IC contains a vertically-recursive and horizontally-transversal filter structure with a filter aperture of eight non-adjacent pixels. Figure 1 is a block diagram of the circuit. The background of the algorithm has been described earlier [1]. The noise level estimation circuit measures the noise in the active video to prevent estimation error due to clean blanking levels inserted by e.g. home recorders. The relationship between the noise estimate and the filter settings can be adapted to the preference of the user.

THE VLSI DESIGN
The new noise reduction IC filters 8-bit digitized luminance and colour-difference signals. The preference of the user is programmed via a UART-like interface. The sampling clock is

![Fig. 1 Block diagram of the TV noise reduction IC](image)

1 The IC is available commercially as SAA4935.
variable up to 16 MHz. The IC includes a split-screen demonstration mode, and can be interfaced to currently-available chipsets for high performance applications including 100 Hz TV with 3-D noise filtering. The 19 mm² chip (Fig.2) is fabricated with a 0.8 μm CMOS process. Further data is presented in Table 1.

<table>
<thead>
<tr>
<th>Table 1. Characteristics of the new IC</th>
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<td>Process</td>
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<td>No. of gates equivalent</td>
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THE PERFORMANCE

A subjective evaluation showed that a gain of nearly 6 dB, over a wide range of input noise levels, can be achieved with the (3-D) cascade of the new design with a classical [2, 3] motion-adaptive temporal noise filter. Experiments also show that about half of this gain is due to the 2-D spatial filter, i.e. the 1-chip economy noise filter, alone. Figure 3 shows the subjective evaluation of the three alternative noise filter concepts. The evaluation was obtained by asking a panel of viewers to try to match two noisy pictures of which one was obtained from the noise filter under test. For details about the test procedure see [1].

CONCLUSIONS

A unique automatically-adaptive economy noise filter for TV was designed and fabricated in silicon. This 1-chip noise reducer yields a gain of about 3 dB in SNR. Cascading the new noise filter with a motion-adaptive 1st-order recursive temporal noise filter as available in current high-end TV sets roughly doubles the noise reduction capabilities of the individual concepts. A total SNR increase of 6 dB results. The interfaces of the new chip match existing chipsets available on the market for high quality TV.

REFERENCES