

Energy reduction using intra-task scenarios†

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Introduction

Portable real-time embedded systems

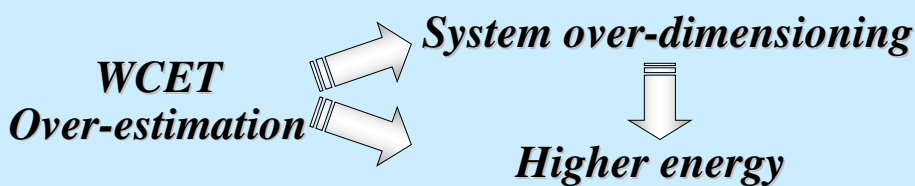
- performance constraints
- low cost
- low energy



Intra-task Scenarios

- A **scenario** is the application behavior for a specific type of input data.
- It incorporates **correlations** between different parts of the application.
- The set of scenarios **must cover** all possible input data.

An example scenario for an MP3 decoder is the application behavior for a mono sample. Together with the scenario for a stereo sample, they cover all possible behaviors.



Method

Automatic Scenario Detection [2,4]

Fully automatic, on static analysis of source code:

- Identifies variables with potential impact on the WCET
- Computes their maximum impact
- Partitions into scenarios based on the variables impact and the comparisons in which the variables appear

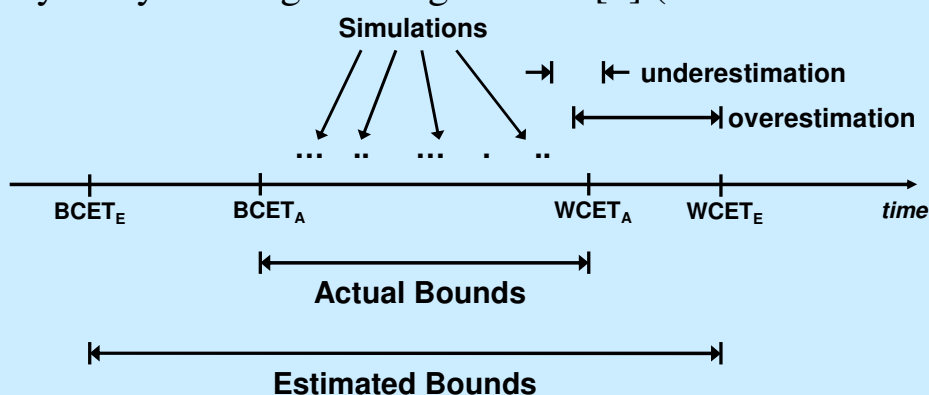
The impact is used to give a good **trade-off** between number of generated scenarios and possible improvement.

WCET Estimation [2]

Worst Case Execution Time (WCET) is affected by:

- The feasible execution paths
- The processor architecture

WCET can be obtained by simulation (**underestimation**) or by analysis using a timing schema [1] (**overestimation**).

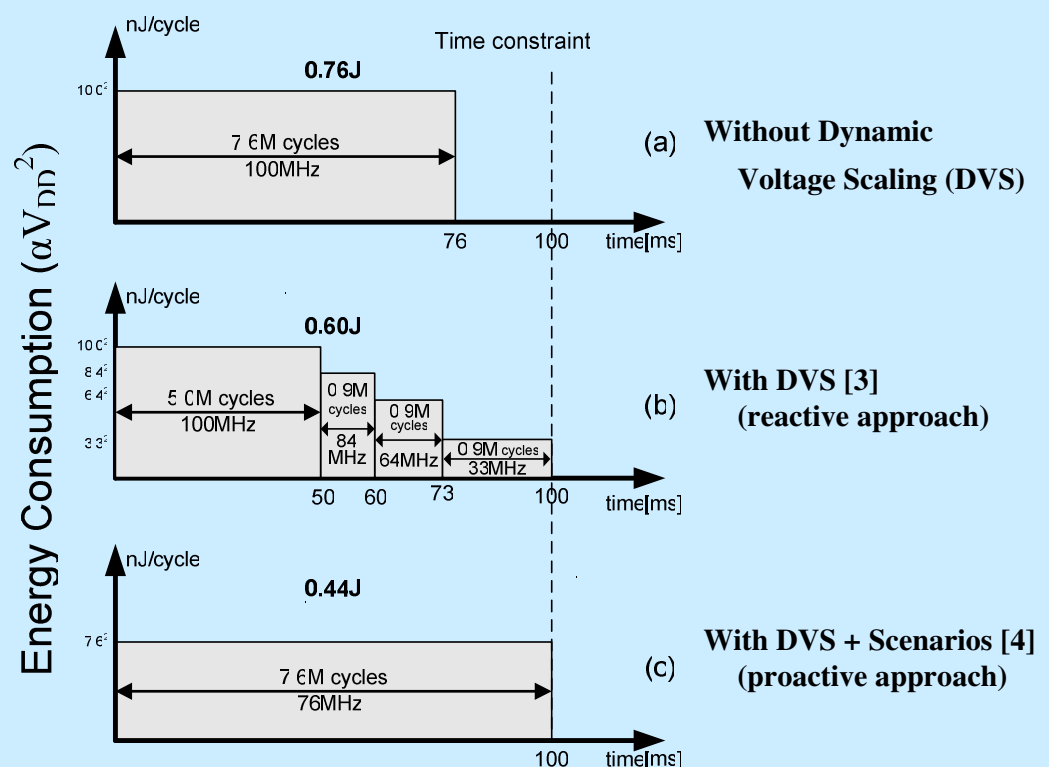


Problem: Timing schema considers also infeasible paths → **overestimation**.

Solution: The scenarios knowledge about correlations is used to reduce the overestimation. The WCET is:

$$WCET(app) = \max_{S \in \text{Scenarios}} (WCET(S))$$

Scenario-aware Voltage Scheduling [4]



In the **proactive** approach, at **runtime** a predictor detects the **scenario** in which the application runs.

Results

	MP3 Decoder	H263 Decoder
WCET reduction	16 %	0 %
Energy reduction	16 %	14 % - 45 %

References

- [1] A. C. Shaw, *Reasoning about Time in Higher-Level Language Software*, IEEE Transactions on Software Engineering, 15(7), pp. 875-889, July 1989.
- [2] S.V. Gheorghita et al., *Automatic Scenario Detection for Improved WCET Estimation*, 42nd IEEE/ACM Design Automation Conference, Proc., pp. 101-104, June 2005, Anaheim, CA, USA.
- [3] D. Shin et al., *Intra-Task Voltage Scheduling for Low-Energy, Hard Real-Time Applications*, IEEE Design & Test of Computers, 18(2), pp. 20-30, March 2001.
- [4] S.V. Gheorghita et al., *Intra-task Scenario-aware Voltage Scheduling*, accepted paper at the ACM International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2005), September 2005, San Francisco, CA, USA.